Part Numbers		OT8502	OT8401	OT8602	OT8200
Host controller		Cortex™ A5 720MHz single core	Cortex™ A5 900MHz single core	Cortex™ A5 900MHz single core	Cortex™ A5 900MHz single core
Video Encoder	H.265 Profile	N.A.	HEVC/H.265 main profile	HEVC/H.265 main profile	N.A.
	H.265 Encoding Performance	N.A.	Line width <= 2048: 120MB/s	Line width <= 2048: 240MB/s Line width > 2048: 200MB/s	N.A.
	H.264 Profile	H.264/MPEG-4 AVC (ISO/IEC 14496-10) baseline, main, and high profile			
	H.264 Encoding Performance	Line width <= 2048: 180MB/s Line width > 2048: 150MB/s	Line width <= 2048: 120MB/s	Line width <= 2048: 240MB/s Line width > 2048: 200MB/s	2MP@60fps
	H.264 ROI Encoding	Up to 8 independent ROI windows. Support different quality and frame rate in each ROI region.			
	MJPEG Performance	120MB/s	Line width <= 2048: 120MB/s	160MB/s	30MB/s
Video Decoder	H.265 Decoding Performance	N.A.	Line width <= 2048: 120MB/s	Line width <= 2048: 240MB/s Line width > 2048: 200MB/s	N.A.
	H.264 Decoding Performance	Line width <= 2048: 180MB Line width > 2048: 150MB	Line width <= 2048: 120MB/s	Line width <= 2048: 240MB/s Line width > 2048: 200MB/s	2MP@60fps
Video Input I/F	Bayer	1*14-bit channel + 1*12-bit channel			2*16-bit channel
	MIPI Rx	1*4-lane channel			
	Sub-LVDS	1*8-lane channel or 2*4-lane channels			N.A.
	BT.1120	2-ch channels			
	BT.656	2-ch (including one MUX-4 channel)			
	BT.601	2-ch			
Max Capture Channel Number		4-ch (up to 1,920 line width for each channel)			
Max Capture Line Width		7936			
Video Output I/F	8-bit BT.656	Support			
	16-bit BT.1120	Support			
	RGB 888	Support			
	sRGB (i80-50MP)	Support			
	MIPI Tx	1*4-lane channel			
	OSD	Up to two OSD layers Support 8/16/32-bit ARGB and 8/16-bit AYUV format Individual chroma keying for each OSD layer			
DRAM		SiP 32-bits 2Gb LPDDR2	SiP 16-bits 1Gb DDR3L	SiP 32-bits 2Gb LPDDR2	SiP 16-bits 512Mb DDR2-1333
NPU		N.A.	0.5 TOPS (1.0 eTOPS)		
Image Signal Processing		Fisheye dewarping correction	N.A.	Fisheye dewarping correction	
		Geometric lens distortion correction			
		Lens shading correction for separated R/G/B component			
		CFA (support Bayer and 2x2 $RGBI_R$ pattern)			
		HDR: multiple shutter frames fusion			
		WDR: local tone mapping			
		Black clamp for separated $R/G_R/B/G_B$ component			
		Fixed pattern noise removal			
		Defect pixel correction			
		Chromatic aberration correction			
		Purple fringe removal			
		Green balance			
		Gamma correction			
		Color correction (2D LUT)			
		Preference color adjustment (3D LUT)			
		Color format conversion			
		Statistic data output for customized 3A process			
		Hue, saturation, and brightness adjustment			
		Contrast enhancement			
		Up to 16x digital gain control for separated $R/G_R/B/G_B$ component			
		Up to 8x white balance gain control for separated $R/G_R/B/G_B$ component			
		2D/3D noise reduction			
		Adaptive weighting edge enhancement			
		Motion detection			
		De-interlace			
		Privacy mask (support arbitray mask shape)			
		Crop, mirror, flip, rotation			
		Resize (support arbitrary scaling ratio from 1/4x to 4x, up to four size-down channels simultaneously)			
Audio Interface		Built-in audio codec Full duplex Single-ended stereo line-in/line-out x1 16/32ohm single-ended stereo headphone-out x1 Mono microphone input x1 Stereo PDM (digital microphone input) I/F x1 I2S I/F x1			I2S I/F x1
USB		USB 2.0 OTG x1			

Ethernet MAC	N.A.	10/100/1000M (support MII / RMII / RGMII; TCP segmentation offload; AVB)		
MMC/SD/SDIO	x2, support up to UHS-1 SDXC; One for SDIO only (compliant with SD version 3.01, SDIO version 3.0, MMC version 4.41, eMMC version 4.0)			
NAND Flash	x1 (compliant with ONFi version 2.2)			
UART	x5 Tx/Rx, or x1 Tx/Rx + x2 with hardware flow control			
ADC	x5, 12-bit resolution, one for on-die temperature measurement			N.A.
I2C	x3			
RTC	x1 (<5uW@3.3V)			N.A.
IrDA	x1			
SPI	x4			
GPIO	Up to 96 bits			
PWM	x12			
XTAL	19.2MHz (for system) and 32.768KHz (for RTC)			19.2Mhz
Boot Device	SPI-NOR, SPI-NAND, NAND, SD, USB, UART			
Clock Generator	5 configurable clock sources (support spread spectrum modulation)			
Security	Support SSLv3 and TLS 1.2 Support up to 256-bit on-chip security key encryption/decryption Up to 640 bits write-only OTP memory and 64 bits read-write OTP memory to store security keys and private information			
Operating Voltage	Core: 1.05V I/O: 1.2 (for LPDDR2)/1.8V/3.3V	Core: 0.9V I/O: 1.2 (for LPDDR2)/1.8V/3.3V		Core: 0.9V I/O: 1.5V / 1.8V / 3.3V
Operating Temperature	-20℃~85℃	-40℃~85℃		
Process	28nm low power			
Package	TFBGA361 (19x19), Ball Pitch: 0.65mm, Dimension: 13mm x 13mm			TFBGA361, Ball Pitch: 0.50mm, Dimension: 9mm x 9mm
Power consumption	~1.0W (including LPDDR2)	~1.0W (including DDR3L)	~1.2W (including LPDDR2)	~0.9W (including DDR2)

OT8xxx Block Diagram